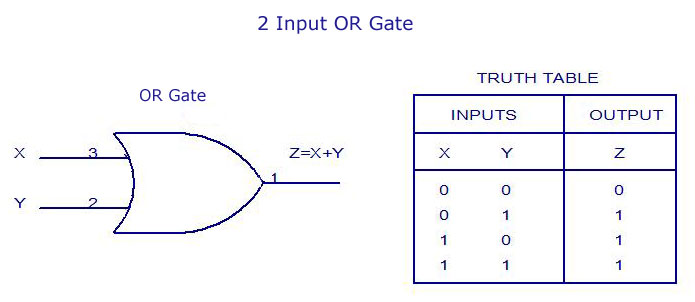
EXPERIMENT NO : 1

NAME : SAHIL TRIPATHI

AIM : Write a Verilog code for the implementation of all gates. –

OR GATE



VERILOG CODE -

module or\_gate(

input a,

input b,

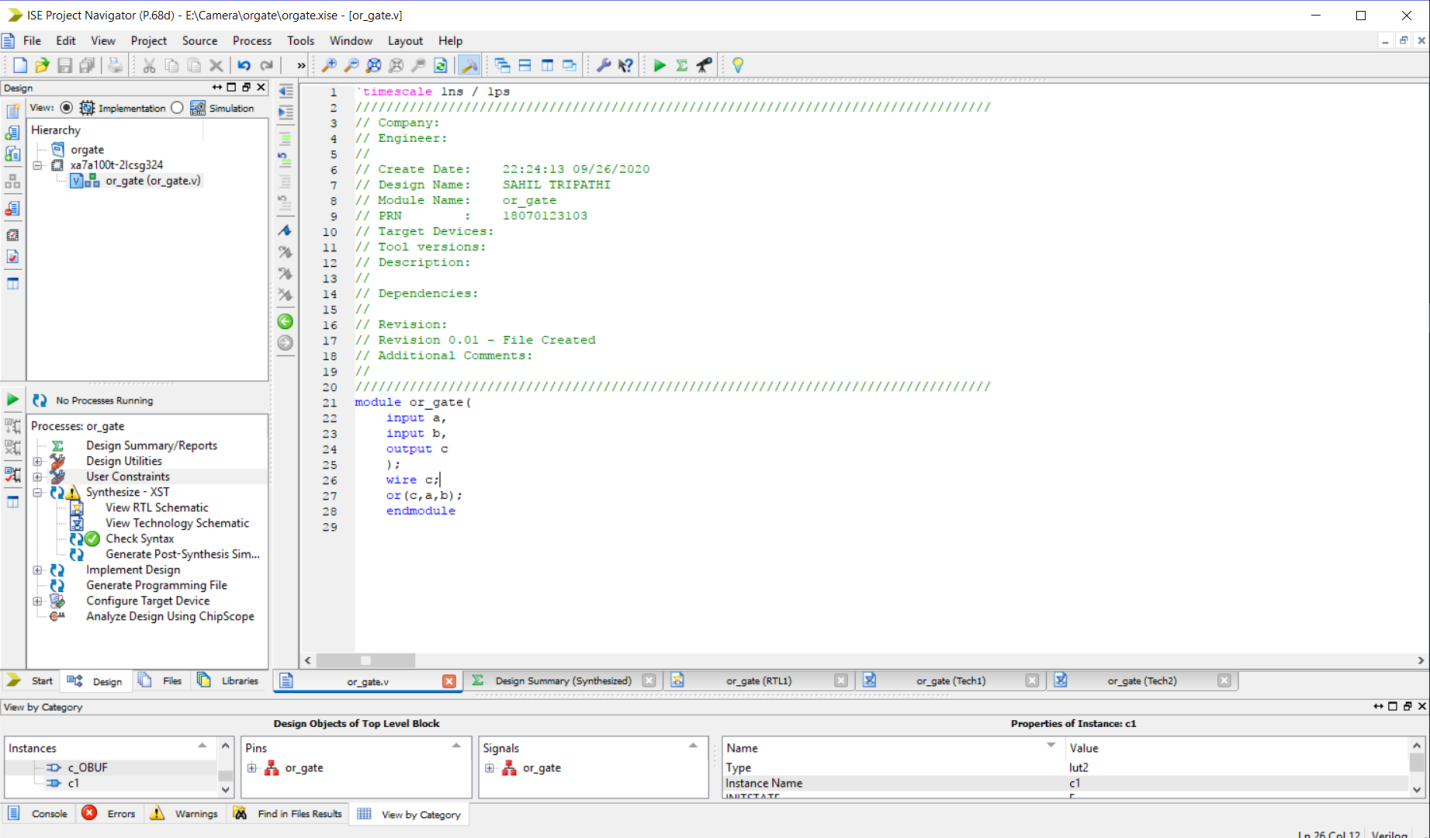
output c

);

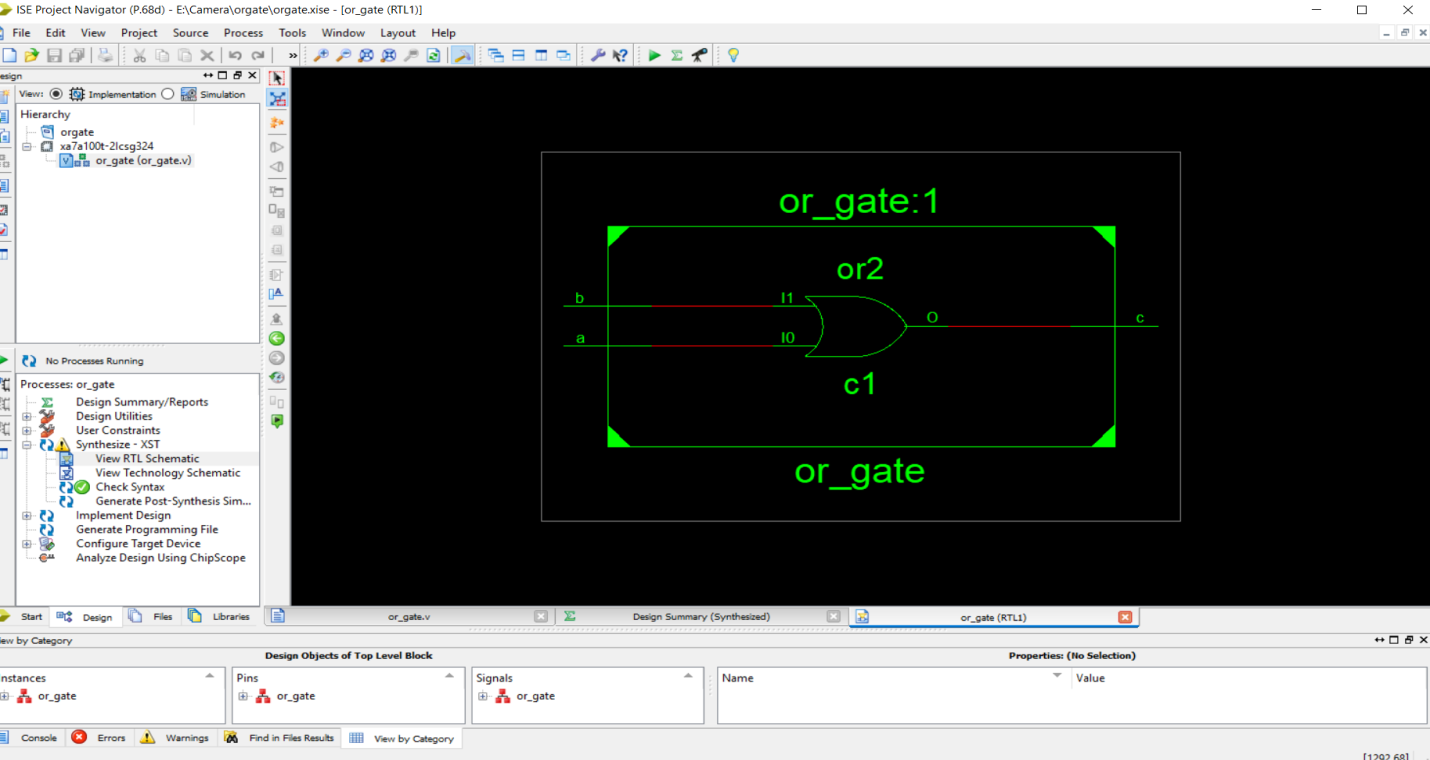
wire c;

or(c,a,b);

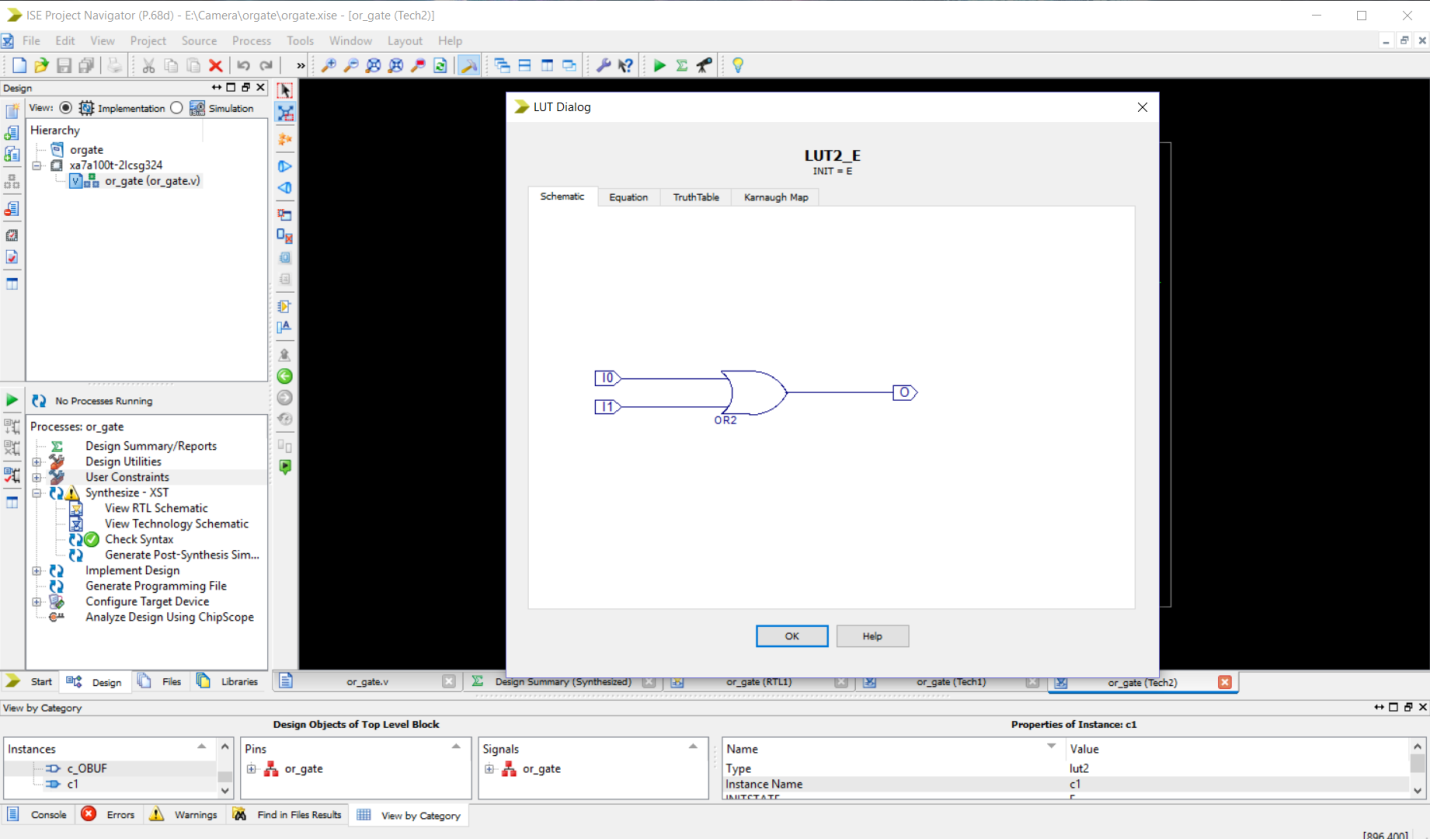
endmodule

IMAGE OF CODE -

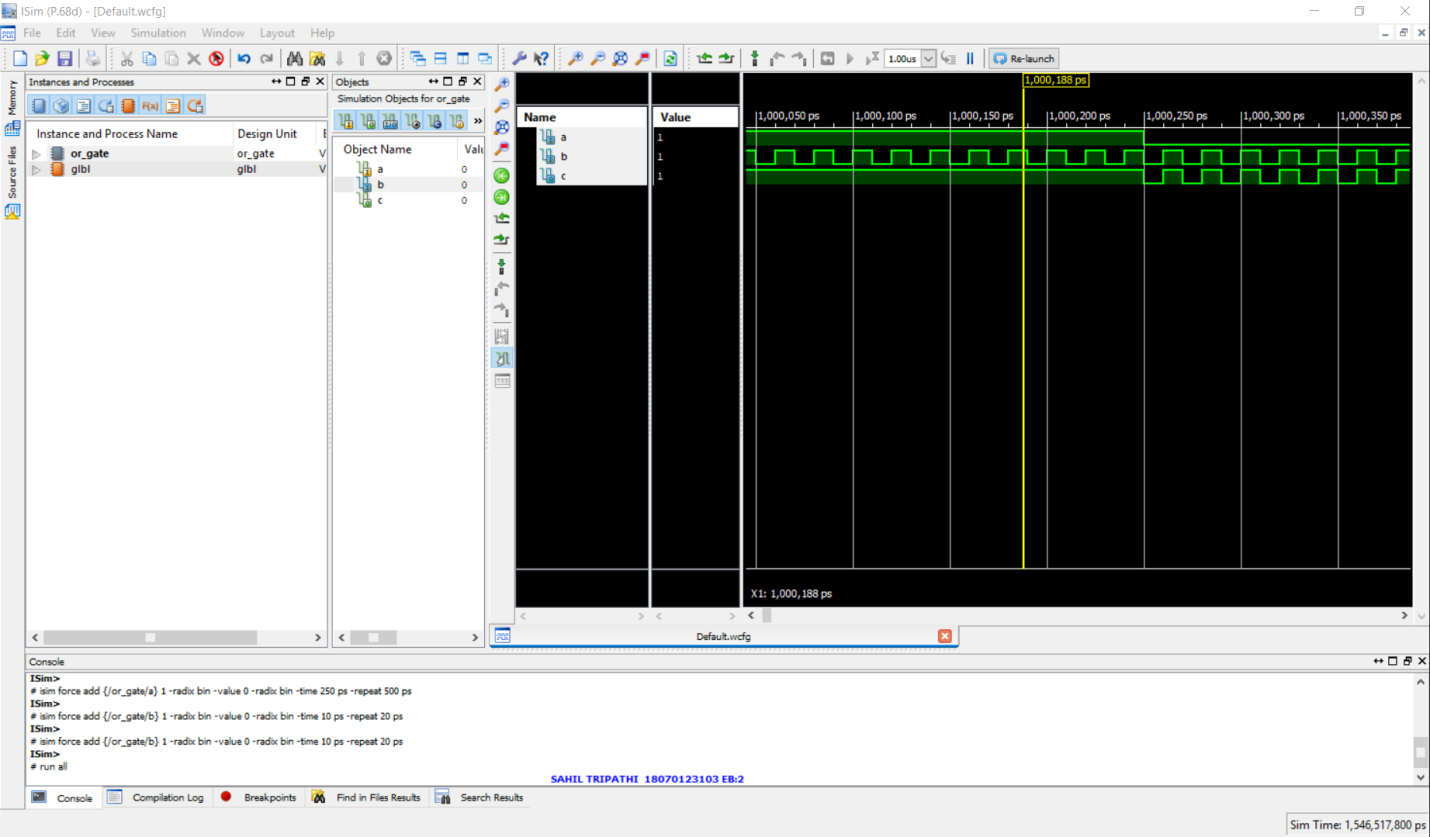
RTL IMAGE OF OR GATE-



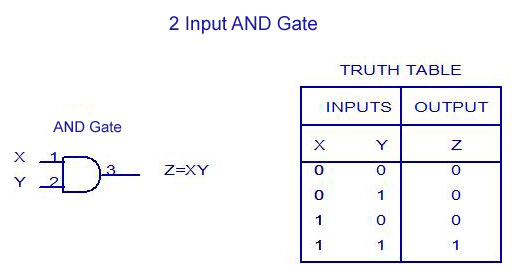
TECHNOLOGY SCHEMATICS



SIMULATION OF OR GATE



## AND GATE



CODE FOR AND

module basicgate(

input a,

input b,

output c

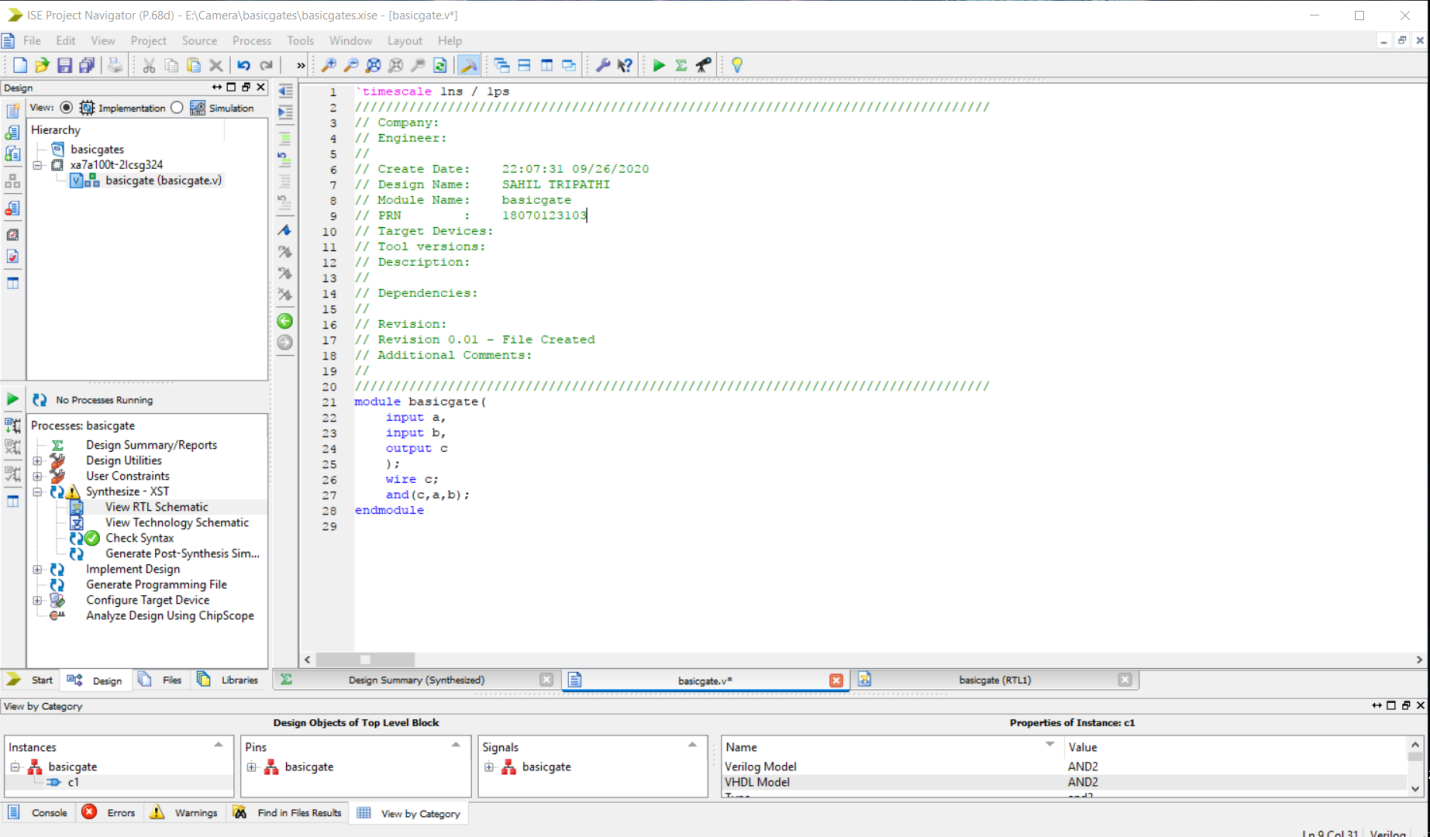
);

wire c;

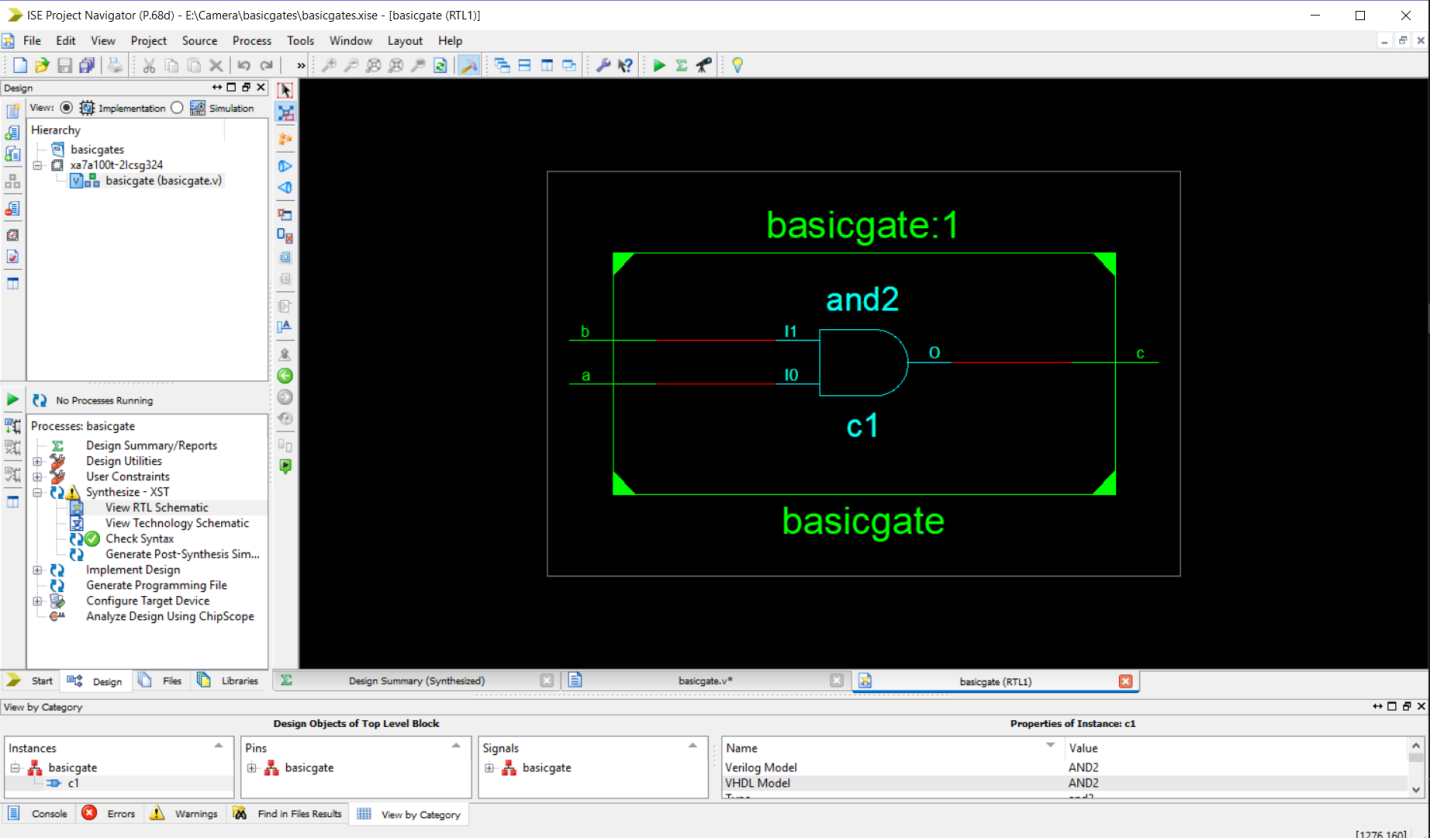
and(c,a,b);

endmodule

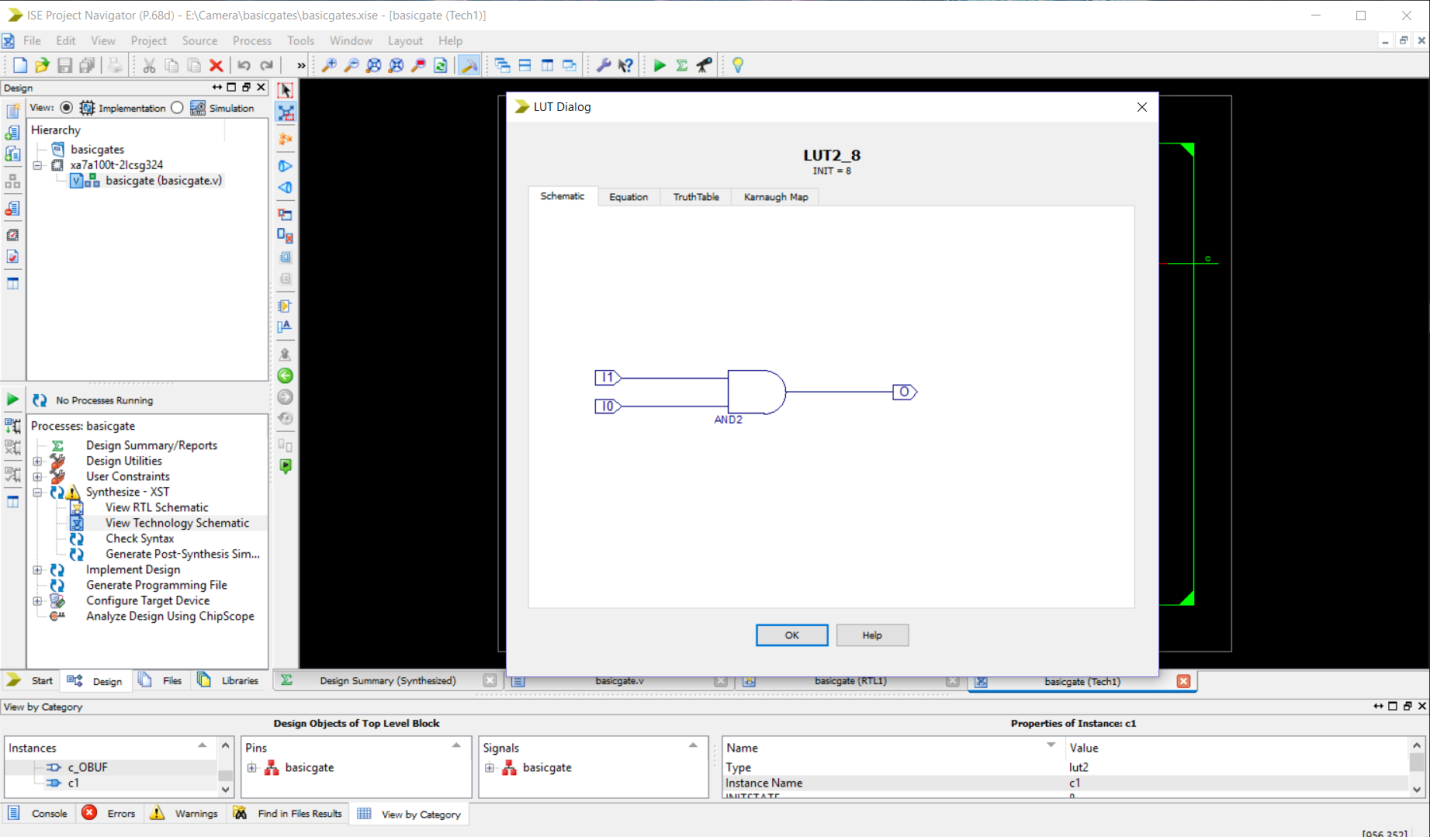
IMAGE OF CODE –



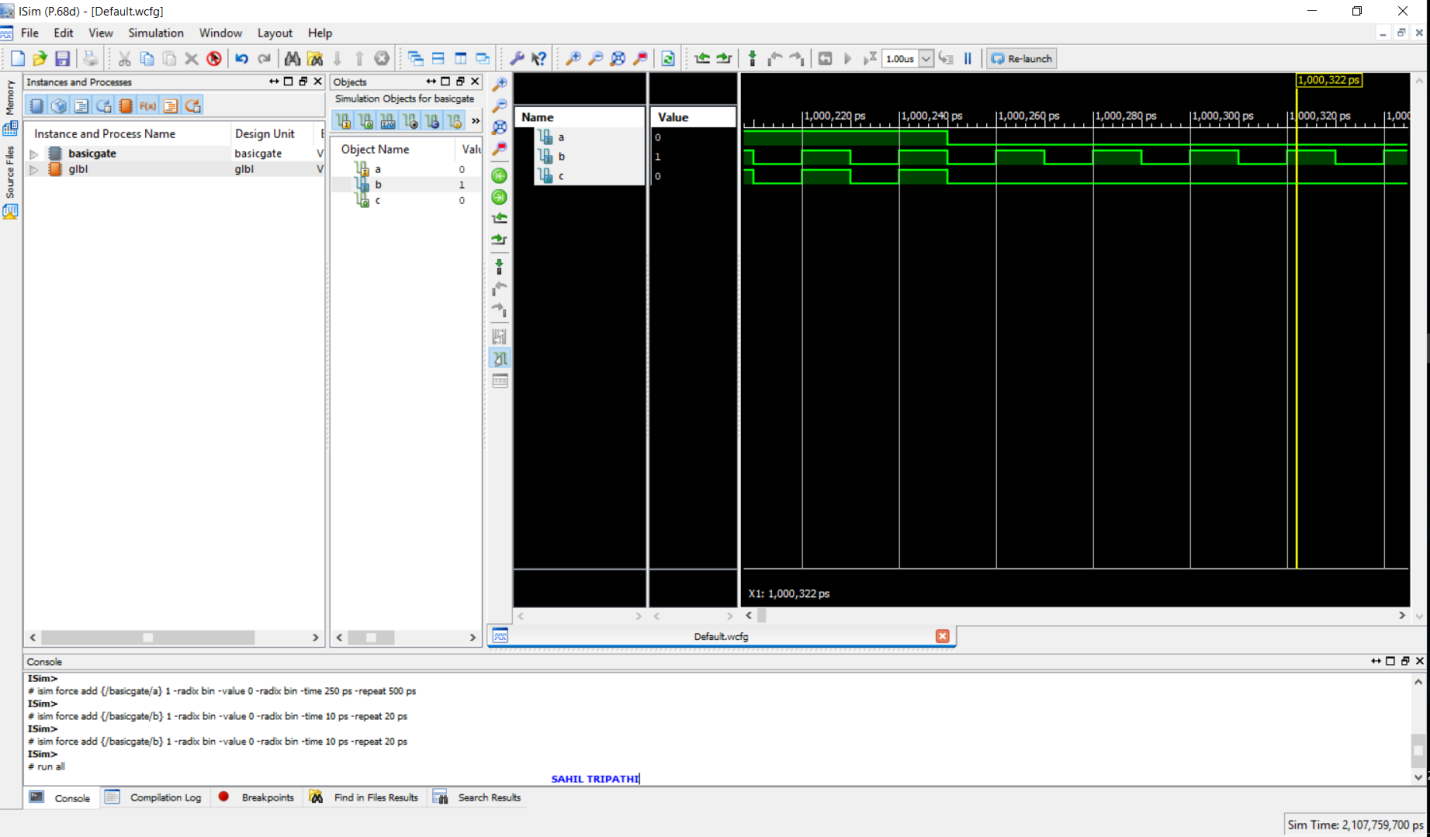
RTL IMAGE OF AND



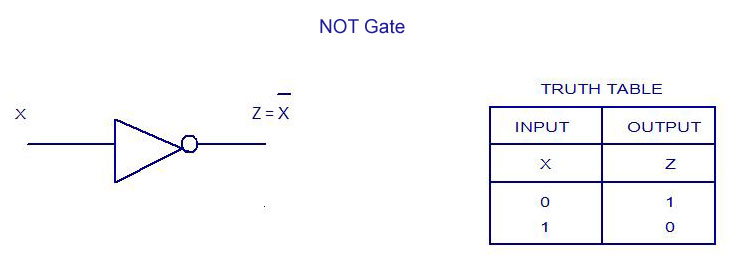
TECHNOLOGY SCHEMATICS



SIMULATION OF AND



## NOT GATE



CODE FOR NOT GATE

module NOT\_GATE(

input a,

output b

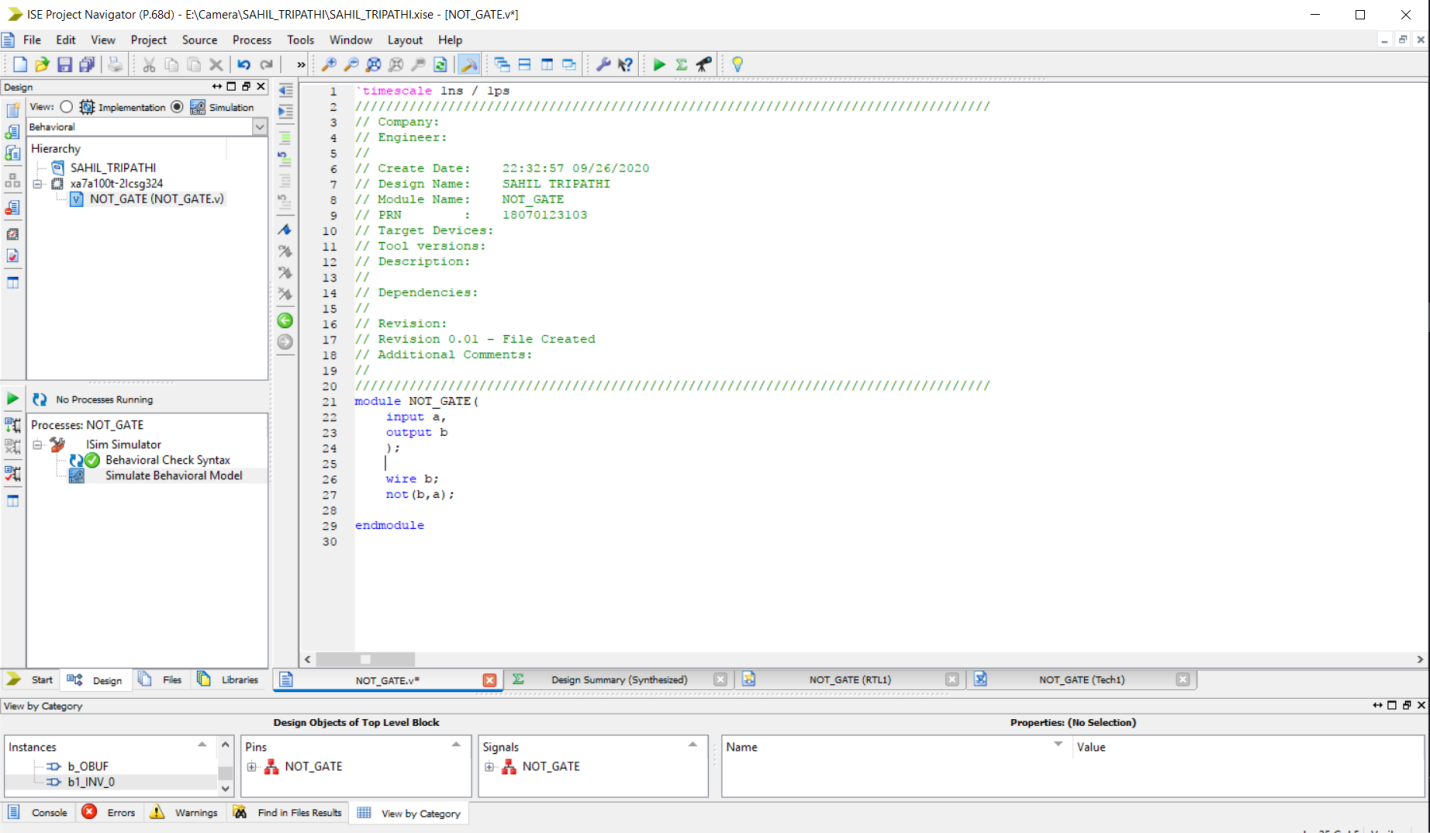
);

wire b;

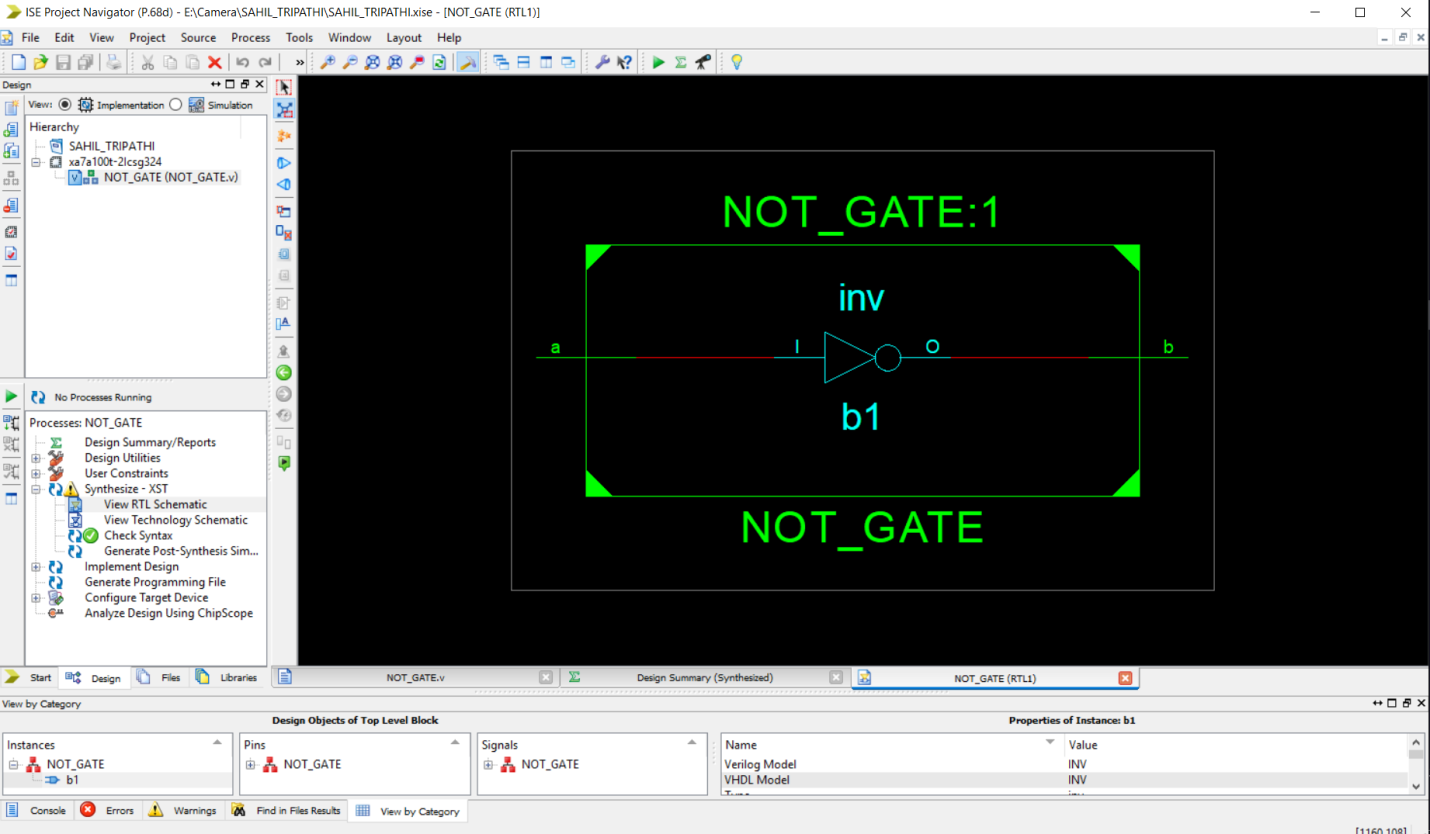
not(b,a);

endmodule

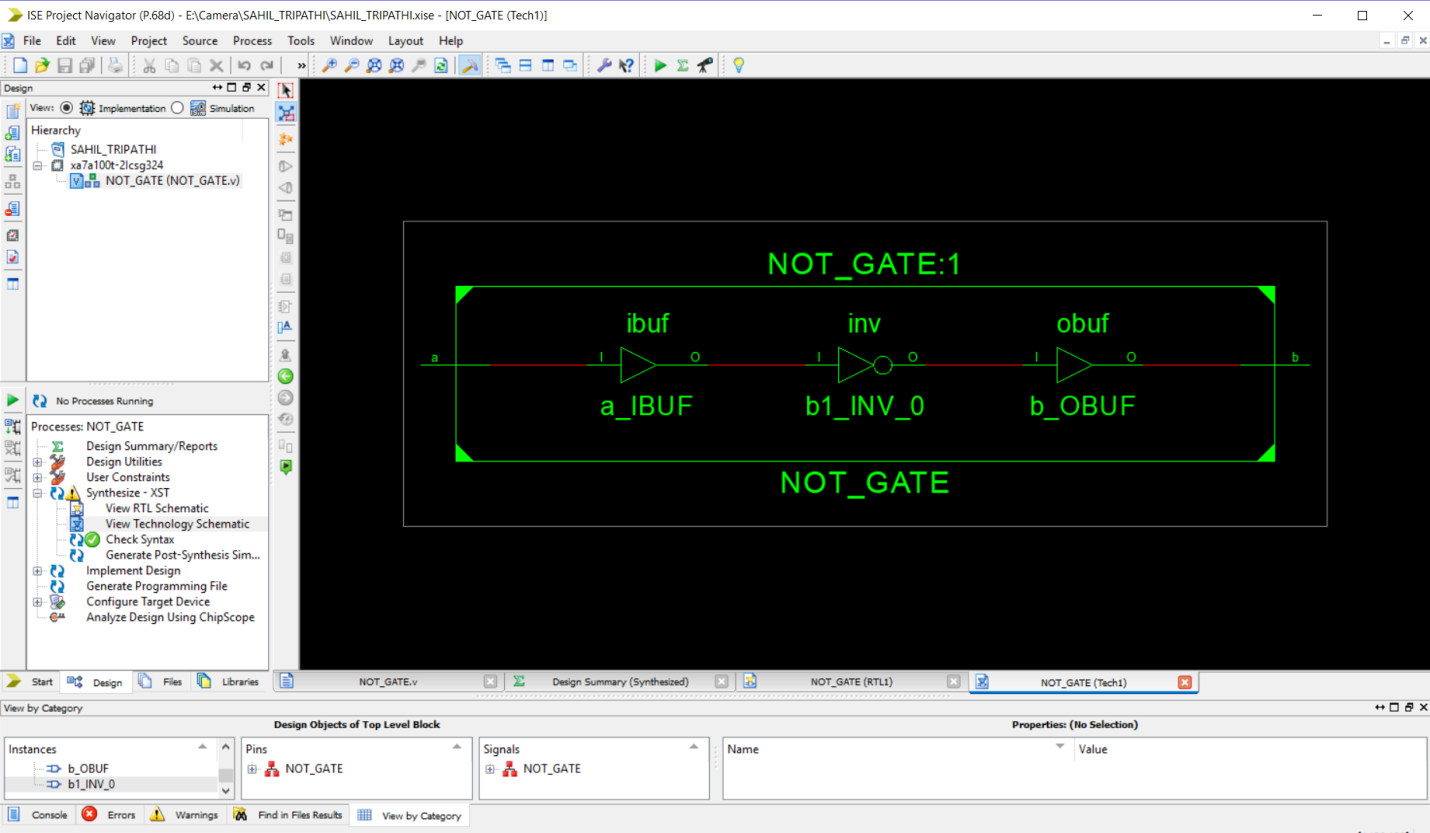
IMAGE FOR CODE-



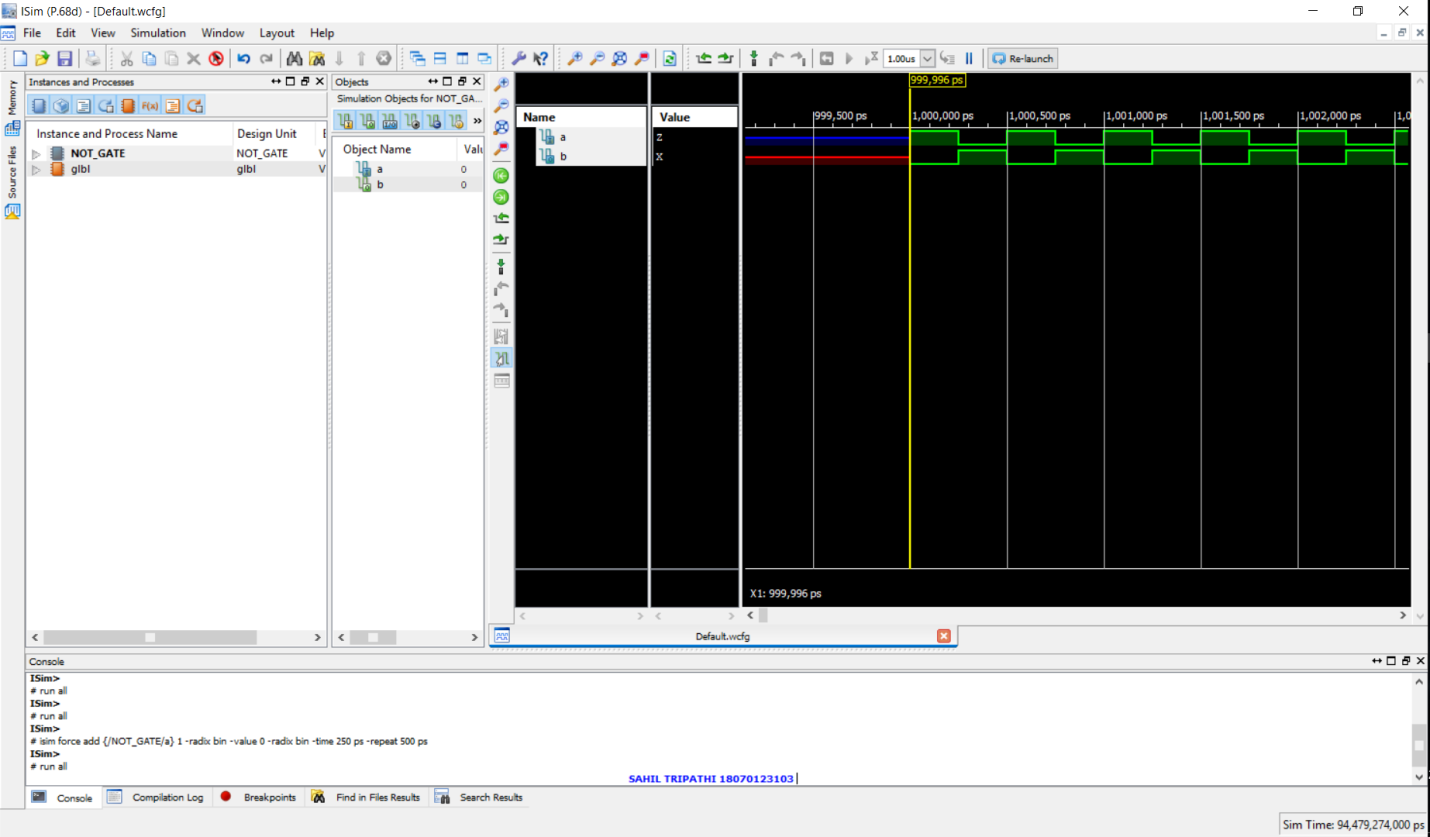
RTL OF NOT GATE



TECHNOLOGY SCHEMATICS



SIMULATION OF NOT



SO HENCE WE HAVE LEARNED HOW TO IMPLEMENT LOGIC GATES & SIMULATE IN XILIN SOFTWARE .